User's Guide

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For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

AgilentE2459A Analysis Probe for MC68040/040V/060

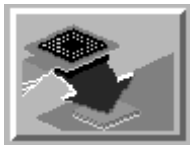
The E2459A Analysis Probe — At a Glance

The E2459A Analysis Probe provides a complete interface for state or timing analysis between any of the supported MC68040/060 microprocessors listed below and logic analyzers. The supported logic analyzers are listed in chapter 1.

Supported Microprocessors

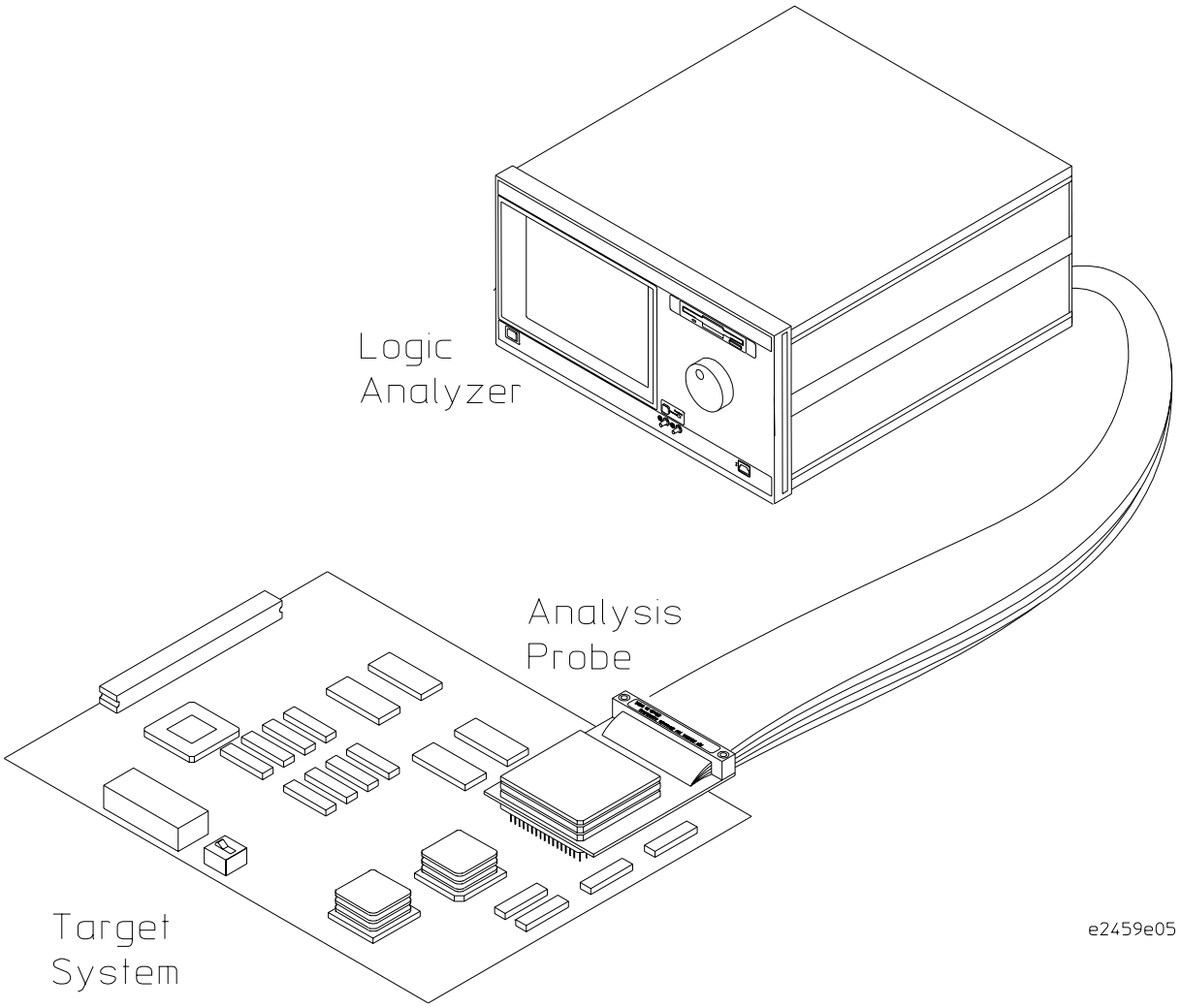
Microprocessor	Package	Ordering Information
68040, 68EC040, 68LC040	179-pin PGA	E2459A
68EC040, 68LC040	184-pin PQFP	E2459A and E5345A
68040V, 68EC040V	182-pin PGA	E2459A
68040V, 68EC040V	184-pin PQFP	E2459A and E5345A
68060, 68EC060, 68LC060	206-pin PGA	E2459A

The analysis probe provides the physical connection between the target microprocessor and the logic analyzer. The configuration software on the enclosed disks set up the logic analyzer for compatibility with the analysis probe. The inverse assemblers on the disks provide displays of the 68040/060 data in 68040/060 assembly language mnemonics.



If you are using the analysis probe with the 16600 or 16700 series logic analysis systems, you only need this manual as a reference. The 16600 and 16700 series contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of Setup Assistant, refer to Chapter 1, "Setup Assistant."

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manuals for those products.

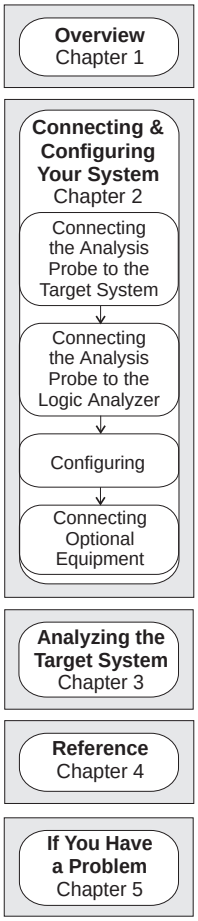


Analyzing a Target System with the E2459A Analysis Probe

In This Book

This book is the User's Guide for the E2459A Analysis Probe. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into the following chapters:



Chapter 1 contains overview information, including a list of required equipment.

Chapter 2 explains how to connect the logic analyzer to your target system through the analysis probe, and how to configure the analysis probe and logic analyzer to interpret target system activity. The last section in this chapter shows you how to hook up optional equipment to obtain additional functionality.

16600 and 16700 Series Logic Analysis Systems

If you are using the analysis probe with 16600 or 16700 series logic analysis systems, you only need this manual as a reference for obtaining and interpreting data. The 16600 and 16700 contain a Setup Assistant, which guides you through the connection and configuration process using on-screen dialog windows. For an overview of Setup Assistant, refer to chapter 1, "Setup Assistant."

Chapter 3 provides information on analyzing the supported microprocessors.

Chapter 4 contains reference information on the analysis probe.

Chapter 5 contains troubleshooting information.

Contents

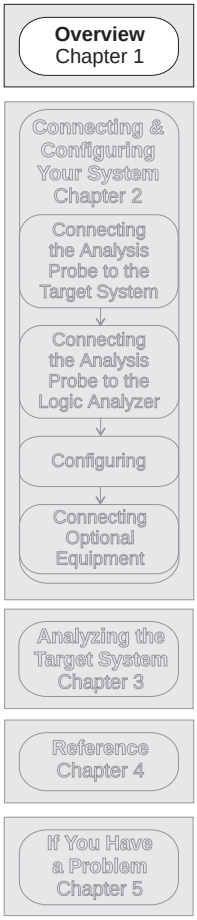
1

Overview

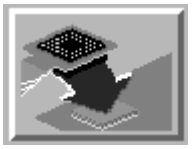
Overview

This chapter describes:

- Setup Assistant
- Logic analyzers supported
- Logic analyzer software version requirements
- Equipment used with the analysis probe
- Equipment supplied
- Minimum equipment required
- Additional equipment supported



Setup Assistant



Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. Setup Assistant is available on the 16600 and 16700 series logic analysis systems. You can use Setup Assistant in place of the connection and configuration procedures provided in chapter 2.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an analysis probe, an emulation module, or other supported equipment. It will also guide you through connecting an analysis probe to the target system.

Access Setup Assistant by clicking its icon in the Logic Analysis System window. The on-screen dialog prompts you to choose the type of measurements you want to make, the type of target system, and the associated products that you want to set up.

If you ordered this product with your 16600/700 logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, this product might not be listed under supported products. In that case, you need to install the M68040-060 Processor Support Package. Use the procedure on the CD-ROM jacket to install the M68040-060 Processor Support Package.

Logic Analyzers Supported

The table below lists the logic analyzers supported by the E2459A analysis probe. Logic analyzer software version requirements are shown on the following page.

The E2459A requires six logic analyzer pods (102 channels) for inverse assembly. The analysis probe contains two additional pods that you can monitor.

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16600A	204	100 MHz	125 MHz	64 k states
16601A	136	100 MHz	125 MHz	64 k states
16602A	102	100 MHz	125 MHz	64 k states
16550A (one or two cards)	102/card	100 MHz	250 MHz	4 k states
16554A (two cards)	68/card	70 MHz	125 MHz	512 k states
16555A (two cards)	68/card	110 MHz	250 MHz	1 M states
16555D (two cards)	68/card	110 MHz	250 MHz	2 M states
16556A (two cards)	68/card	100 MHz	200 MHz	1 M states
16556D (two cards)	68/card	100 MHz	200 MHz	2 M states
1660A/AS/C/CS/CP	136	100 MHz	250 MHz	4 k states
1661A/AS/C/CS/CP	102	100 MHz	250 MHz	4 k states
1670A	136	70 MHz	125 MHz	64 k or .5 M states
1670D	136	100 MHz	125 MHz	64 k or 1 M states
1671A	102	70 MHz	125 MHz	64 k or .5 M
1671D	102	100 MHz	125 MHz	64 k or 1 M

Logic analyzer software version requirements

The logic analyzers must have software with a version number greater than or equal to those listed below to make a measurement with the E2459A. You can obtain the latest software at the following web site:

www.agilent.com/

If your software version is older than those listed, load new system software with the above version numbers or higher before loading the E2459A software.

Logic Analyzer Software Version Requirements

Logic Analyzer	Minimum Logic Analyzer Software Version for use with E2459A	
16600 Series	The latest 16600 logic analyzer software version is on the CD-ROM shipped with this product.	
1660A/AS Series	A.03.01	
1660C/CS/CP Series	A.02.01	
1670A/D Series	A.02.01	
Mainframes*		
16700 Series	The latest 16700 logic analyzer software version is on the CD-ROM shipped with this product.	
16500C Mainframe**	A.01.05	A.01.05
16500B Mainframe**	A.03.14	A.03.14

* The mainframes are used with the 16550 and 16554/55/56 logic analyzer modules.

Equipment Used with the Analysis Probe

This section lists equipment used with the analysis probe. This information is organized under the following titles: equipment supplied, minimum equipment required, and additional equipment supported

Equipment supplied

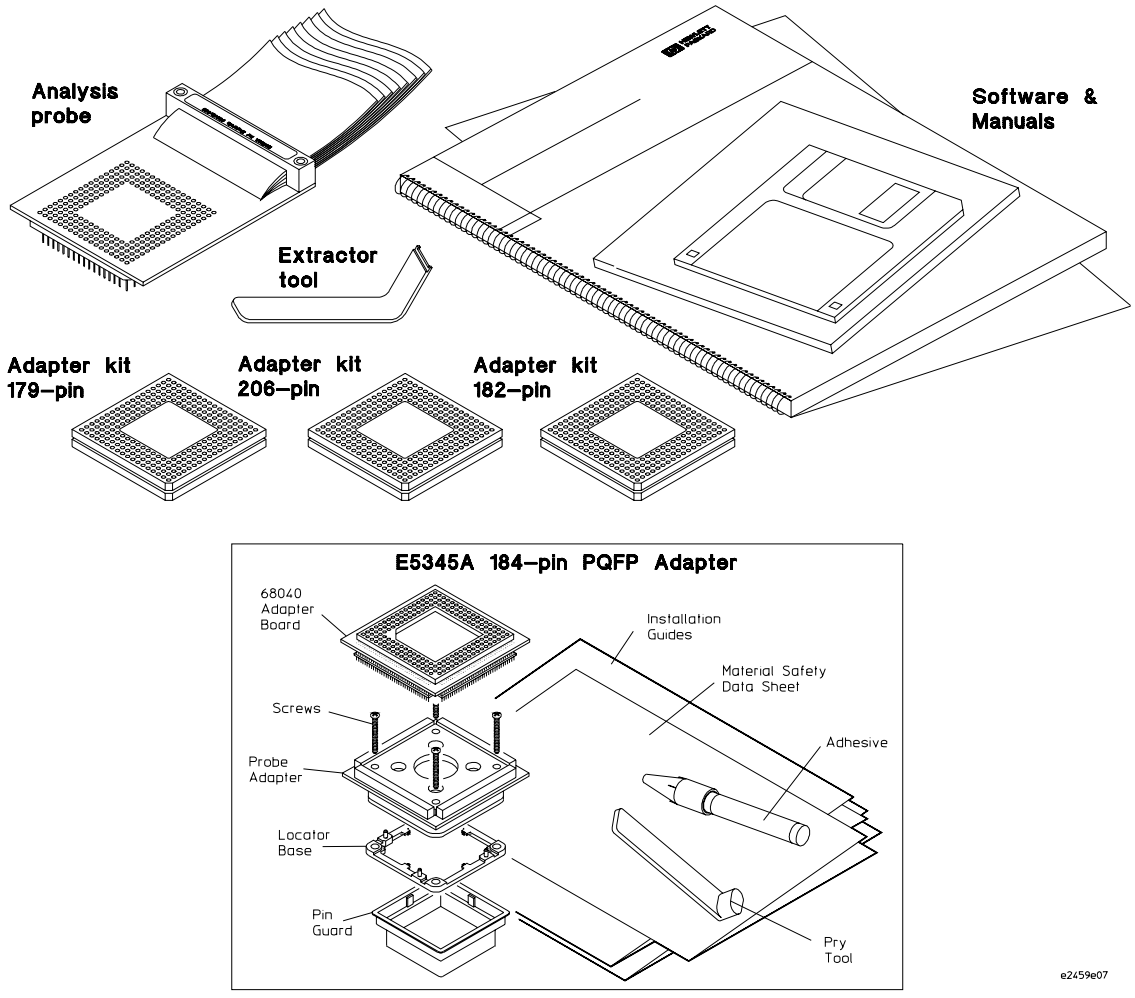
The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below:

E2459A Analysis Probe

- The analysis probe, which includes the analysis probe circuit card and cables.
- Logic analyzer configuration files and inverse assembler software on a 3.5-inch disk.
- Logic analyzer configuration files and inverse assembler software on a CD-ROM.
- Three adapter kits (179-pin, 182-pin, and 206-pin). Each kit contains two sockets.
- An extractor tool, for separating sockets, and a User's Guide.
- This User's Guide.

E5345A 184-pin PQFP Adapter

- 68040 Adapter Board.
- 184-pin PQFP Adapter Assembly.
- Installation Notes (2).



Equipment Supplied with the E2459A

Minimum equipment required

For state and timing analysis of an MC68040/060 target system, you need all of the following items.

- The E2459A Analysis Probe.
- For 184-pin PQFP target systems, the E5345A PQFP Adapter.
- One of the logic analyzers listed on page 1-4. The logic analyzer software version requirements are listed on page 1-5.

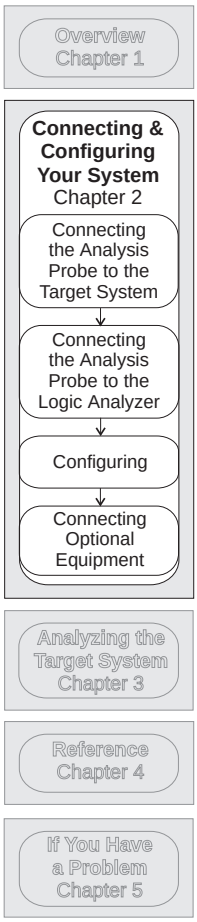
Additional equipment supported

The E2459A does not support any additional equipment.

2

Connecting and Configuring Your System

Connecting and Configuring Your System

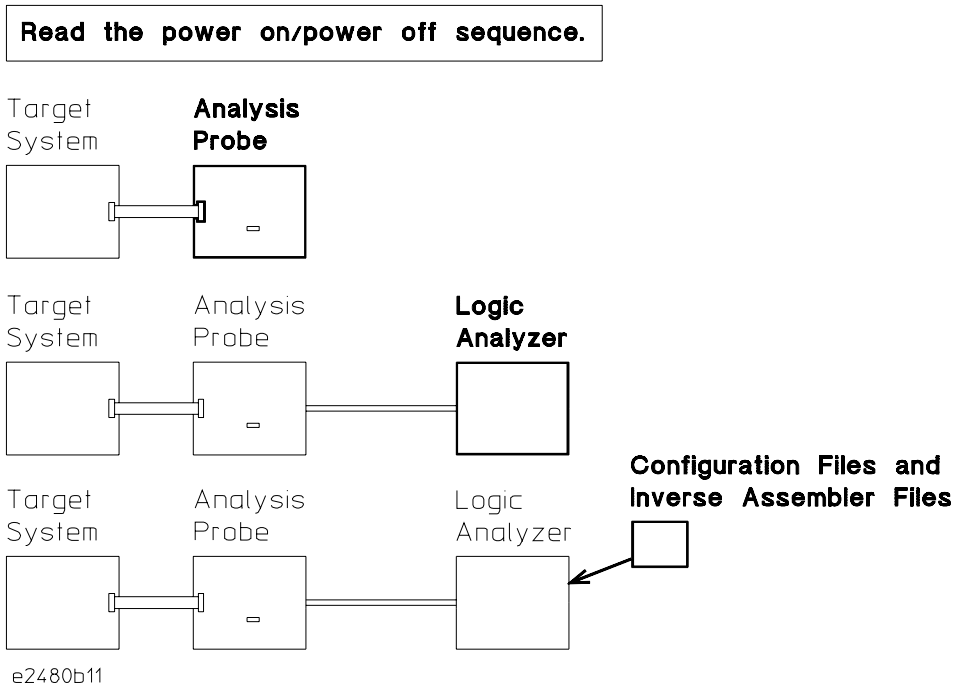


This chapter shows you how to connect the logic analyzer to the target system through the analysis probe.

If you are connecting to an 16600 or 16700 series logic analysis system, follow the instructions given on-screen in the Setup Assistant for connecting and configuring your system. Use this manual for additional information, if desired. Refer to chapter 1 for a description of Setup Assistant.

If you are not using the Setup Assistant, follow the instructions given in this chapter. This chapter is divided into the following sections; the order shown here is the recommended order for performing these tasks:

- Read the power on/power off sequence
- Connect the analysis probe to the target system
- Connect the analysis probe to the logic analyzer
- Configure the logic analyzer
- Connect optional equipment



Connection Sequence

Power-on/Power-off Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

To power on 16600 and 16700 series logic analysis systems

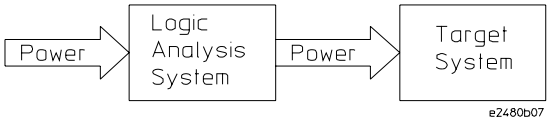
Ensure the target system is powered off.

1. Turn on the logic analyzer. The Setup Assistant will guide you through the process of connecting and configuring the analysis probe.
2. When the analysis probe is connected to the target system and logic analyzer, and everything is configured, turn on your target system.

To power on all other logic analyzers

With all components connected, power on your system in the following order:

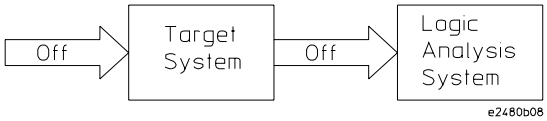
1. Logic analysis system.
2. Your target system.



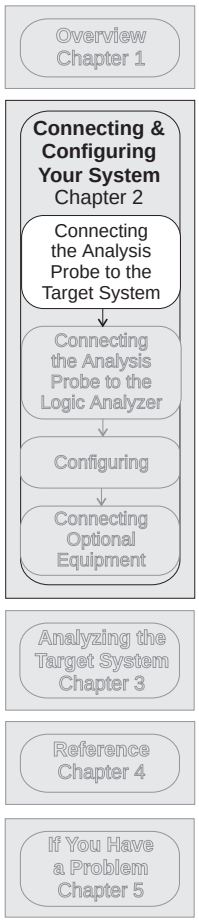
To power off

Turn off power to your system in the following order:

1. Turn off your target system.
2. Turn off your logic analysis system.



Connecting the Analysis Probe to the Target System



This section explains how to connect the E2459A Analysis Probe to the target system. Connecting the analysis probe to the target system consists of the following steps, which are described on the following pages:

- For PGA target systems, attach the appropriate adapter kit to the PGA socket on the bottom of the analysis probe, then connect the analysis probe to the target system.

  Refer to "To connect to a PGA target system."

- For PQFP target systems, connect the probe adapter to the target system, then connect the analysis probe to the probe adapter.

  Refer to "To connect to a PQFP target system."

The remainder of this section describes these general tasks in more detail.

Protect Your Equipment

The analysis probe socket assembly pins are covered for shipment with a conductive foam wafer or conductive plastic pin protector. This protects the delicate gold-plated pins from damage due to impact. When you are not using the analysis probe, protect the socket assembly pins by covering them with the pin protector.

To connect to a PGA target system

CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

1. Turn off the target system and disconnect all logic analyzer cables from the analysis probe.
2. Remove the 68040/040V/060 PGA microprocessor from its socket on the target system and store it in a protected environment.
3. Attach the appropriate PGA adapter kit socket to the PGA socket on the bottom of the analysis probe. Ensure that the adapter kit pin A1 corner (notched) is aligned with the analysis probe pin A1 corner (also notched). See figure on next page.

   Apply even pressure around the socket to minimize the possibility of bending or breaking the pins on the analysis probe when removing an adapter.

NOTE

When removing the protective foam covering the analysis probe socket pins, be sure the plastic insulator remains in place.

4. Carefully align the analysis probe connector with the socket on the target system so that all pins are making contact.

CAUTION

Note the position of pin A1 on the analysis probe and microprocessor prior to making any connection. Also, take care to align the analysis probe connector with the target system socket so that all pins are making contact.

5. Plug the analysis probe connector into the microprocessor socket on the target system.

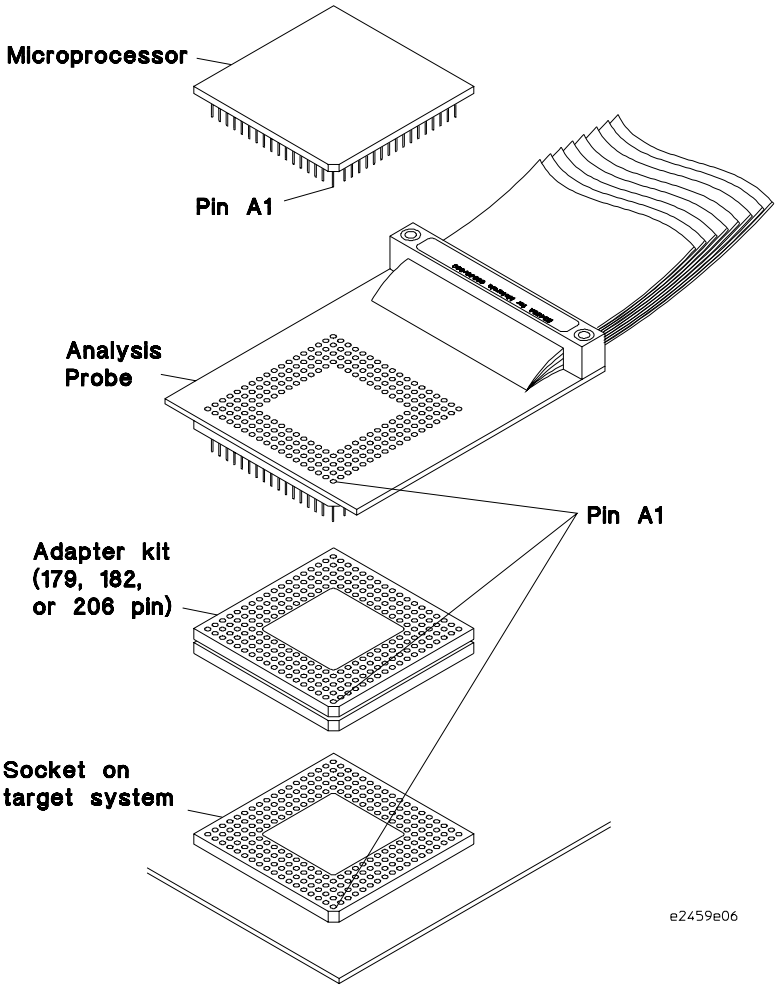
NOTE

If the analysis probe connector interferes with components of the target system or if a higher profile is required, additional plastic pin guards can be added. Plastic pin guards can be ordered from Hewlett-Packard using the part numbers 1200-1910 for the 68040, 1200-1908 for the 68040V, and 1200-1906 for the 68060.

6. Plug the 68040/040V/060 microprocessor into the socket of the analysis probe board. The socket on the analysis probe board is designed with low-insertion-force pins to allow you to install or remove the microprocessor with a minimum amount of force.

CAUTION

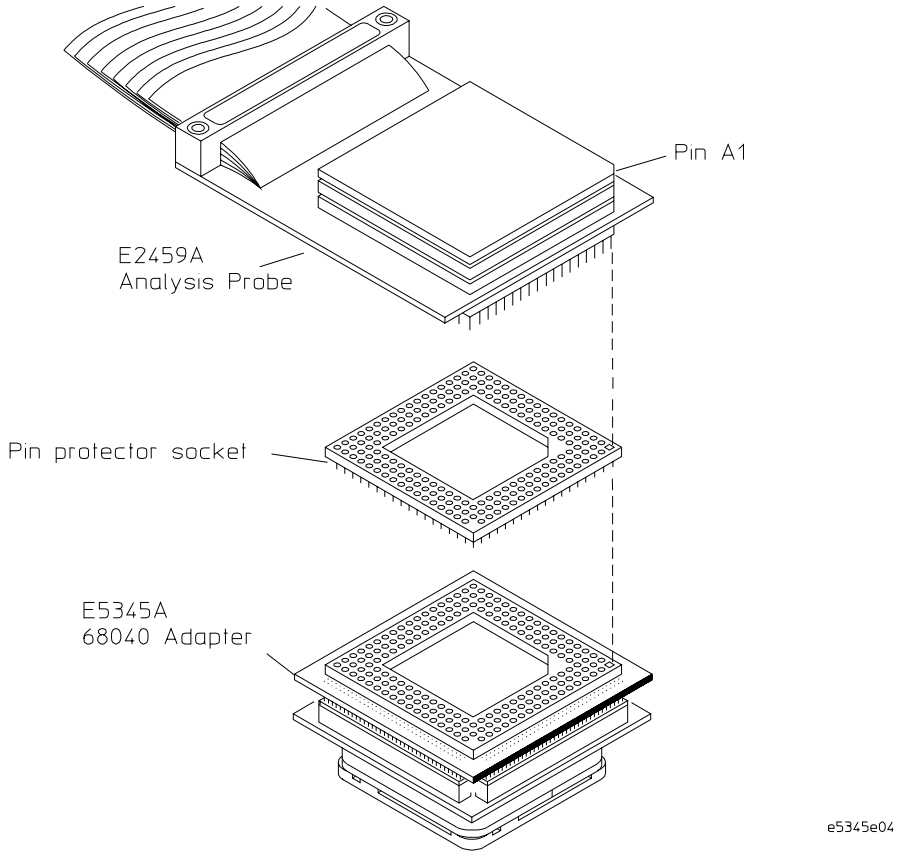
Care must be used when removing a microprocessor or socket from the analysis probe board to prevent damaging the traces on the board.



Pin A1 Location

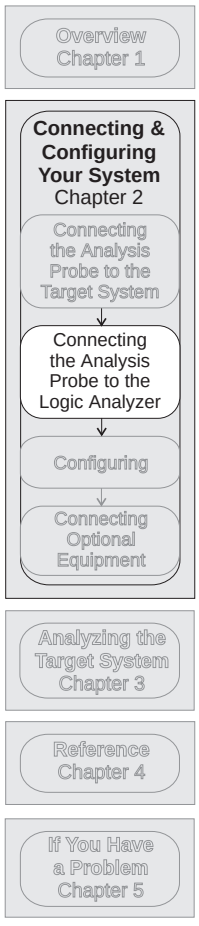
To connect to a PQFP target system

With the E5345A adapter, you can connect to a PQFP microprocessor (see below). For PQFP target systems, use the instructions in the "E5345A 68040 Adapter Installation Note" to connect the adapter to the target system microprocessor. You do not have to remove the target system microprocessor, and you do not need a PGA microprocessor on top of the analysis probe. Ensure that pin 1 is properly aligned.



PQFP Connections

Connecting the Analysis Probe to the Logic Analyzer



The following sections show the connections between the logic analyzer pod cables and the analysis probe cables. Use the appropriate section for your logic analyzer. The configuration file names for each logic analyzer are located at the bottom of the connection diagrams.

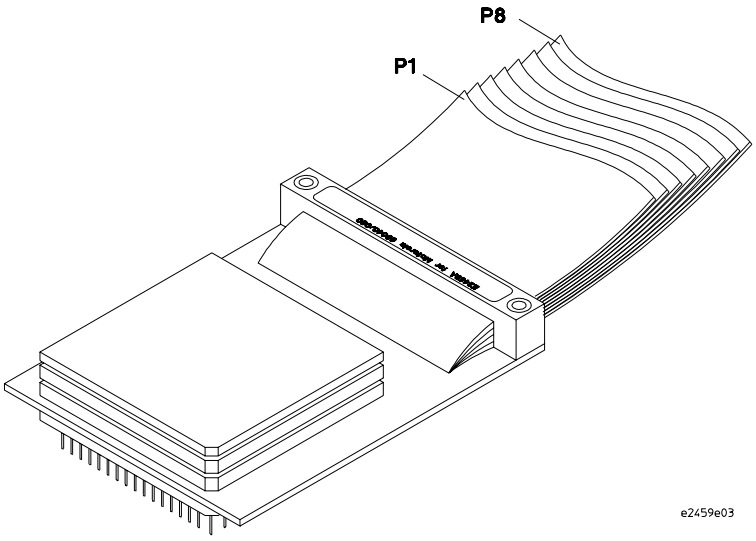
A minimum of six analysis probe pods are required for inverse assembly (P1, P2, P3, P4, P5, and P6). P7 and P8 contain additional signals you might want to monitor. The illustration on the following page shows the pod locations on the analysis probe.

This section shows connection diagrams for connecting the analysis probe to the logic analyzers listed below:

- 16600A logic analysis system
- 16601A logic analysis system
- 16602A logic analysis system
- 16550A logic analyzers (one or two cards)
- 16554/55/56 logic analyzers (two cards)
- 1660A/AS/C/CS/CP logic analyzers
- 1661A/AS/C/CS/CP logic analyzers
- 1670A/D logic analyzers
- 1671A/D logic analyzers

Analysis probe pod locations

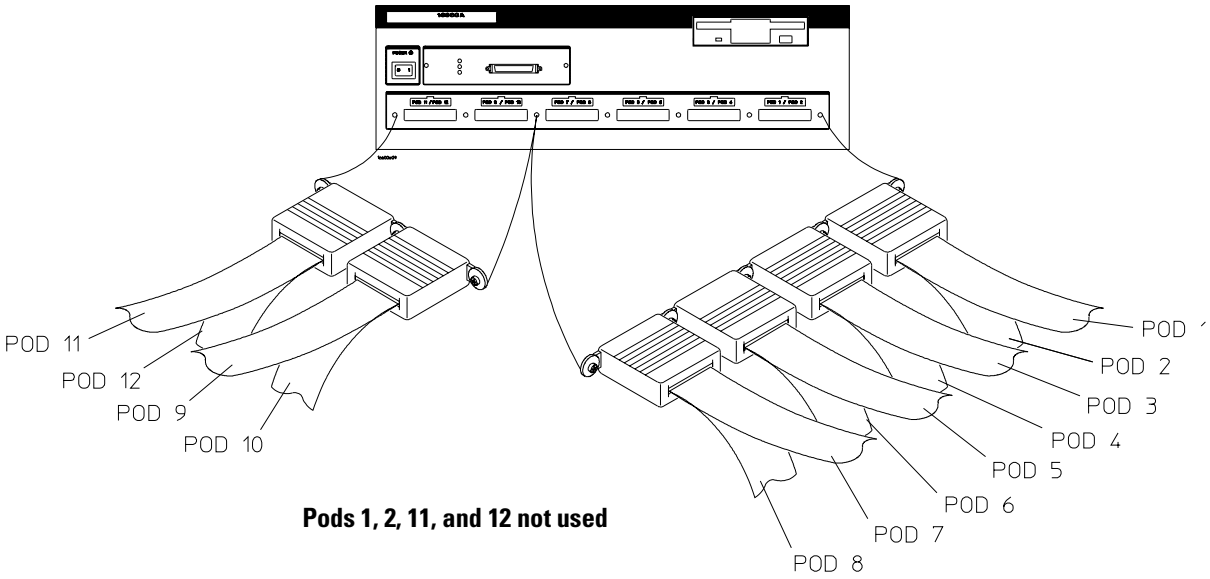
The illustration below shows the pod locations on the analysis probe.



E2459A Analysis Probe Pod Locations

To connect to the 16600A logic analysis system

Use the figure and table below to connect the analysis probe to the 16600A logic analysis system.



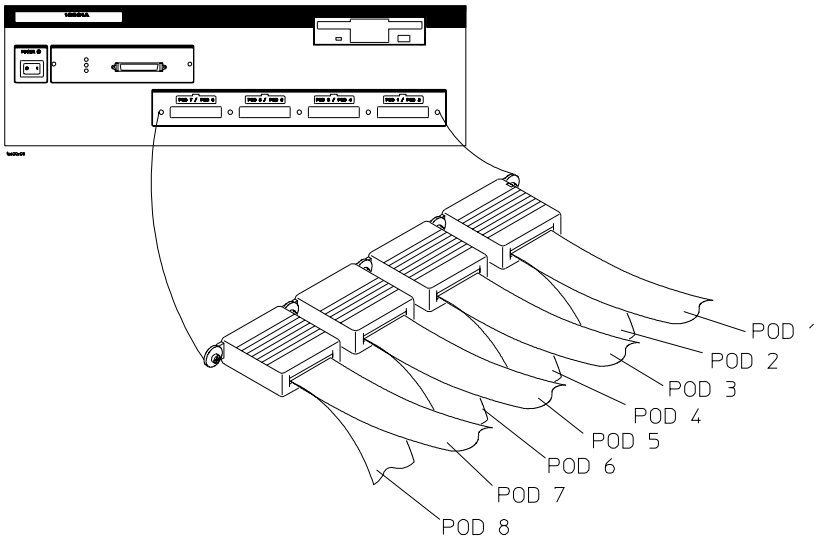
Pods 1, 2, 11, and 12 not used

16600	Pod 10	Pod 9	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3
E2459A Connector	P8 jtag	P7 busarb	P6 STAT	P5 STAT	P4 DATA	P3 DATA	P2 ADDR clk ↑ (68040)	P1 ADDR clk ↑ (68060)

Configuration File
Use configuration files C040F2 or C060F2 for the 16600 logic analysis system.

To connect to the 16601A logic analysis system

Use the figure and table below to connect the analysis probe to the 16601A logic analysis system.

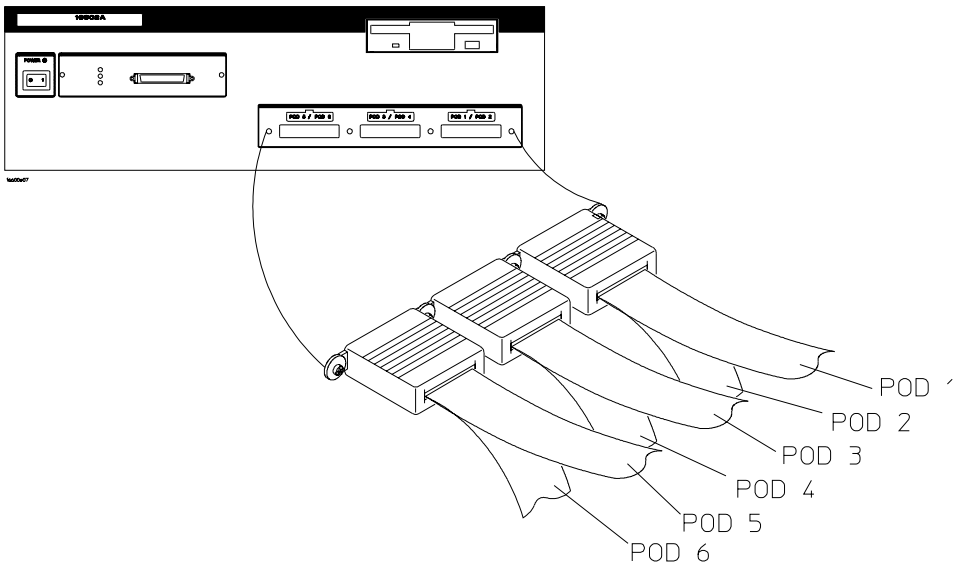


16601	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
E2459A Connector	P6 STAT	P5 STAT	P4 DATA	P3 DATA	P2 ADDR clk ↑ (68040)	P1 ADDR clk ↑ (68060)	P8 jtag	P7 busarb

Configuration File
Use configuration files C040F2 or C060F2 for the 16601 logic analysis system.

To connect to the 16602A logic analysis system

Use the figure and table below to connect the analysis probe to the 16602A logic analysis system.

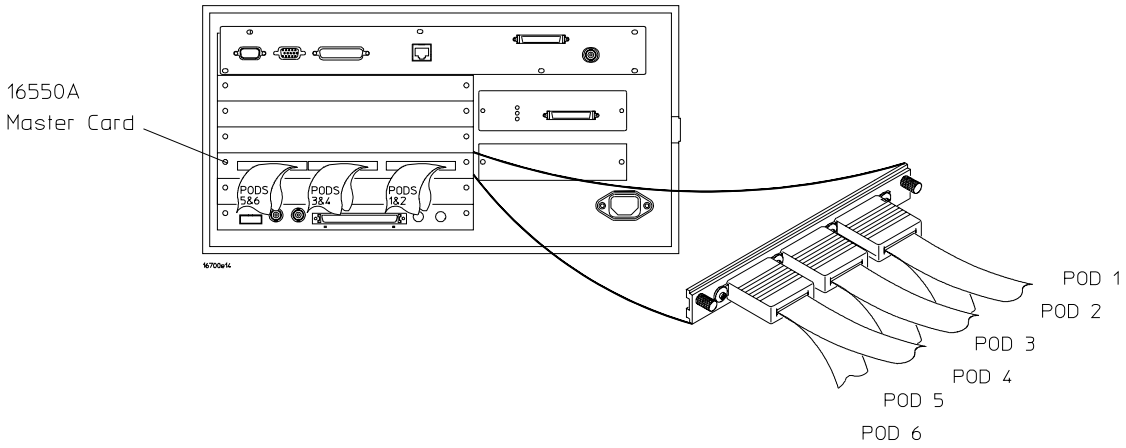


16602	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
E2459A Connector	P6 STAT	P5 STAT	P4 DATA	P3 DATA	P2 ADDR clk ↑ (68040)	P1 ADDR clk ↑ (68060)

Configuration File
Use configuration files C040F2 or C060F2 for the 16602 logic analysis system.

To connect to the one-card 16550A logic analyzer

Use the figure and table below to connect the analysis probe to the one-card 16550A logic analyzer.

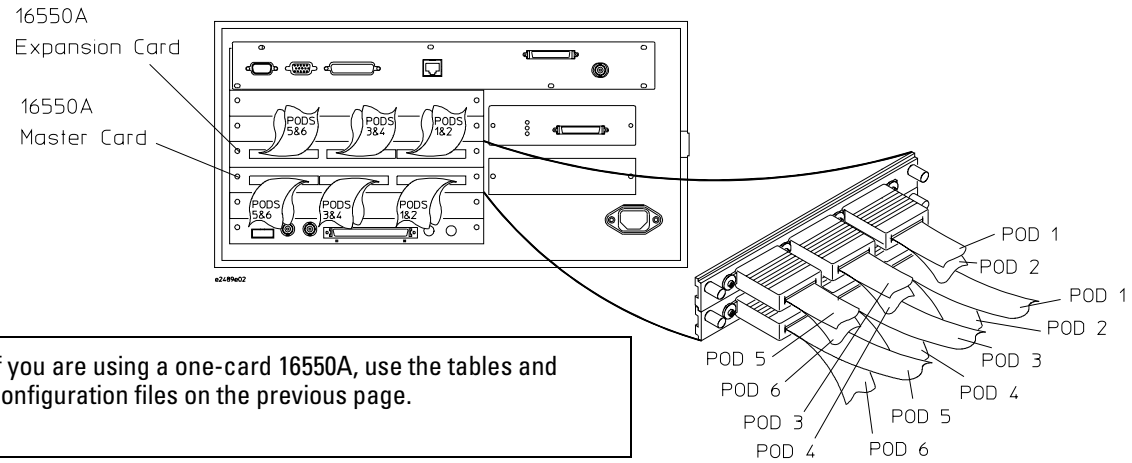


16550A Master Card	Master Card Pod 6	Master Card Pod 5	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
E2459A Connector	P6 STAT	P5 STAT	P4 DATA	P3 DATA	P2 ADDR clk ↑ (68040)	P1 ADDR clk ↑ (68060)

Configuration File
Use configuration files C040F or C060F for the one-card 16550A logic analyzer.

To connect to the two-card 16550A logic analyzer

Use the figure and table below to connect the analysis probe to the two-card 16550A logic analyzer.



If you are using a one-card 16550A, use the tables and configuration files on the previous page.

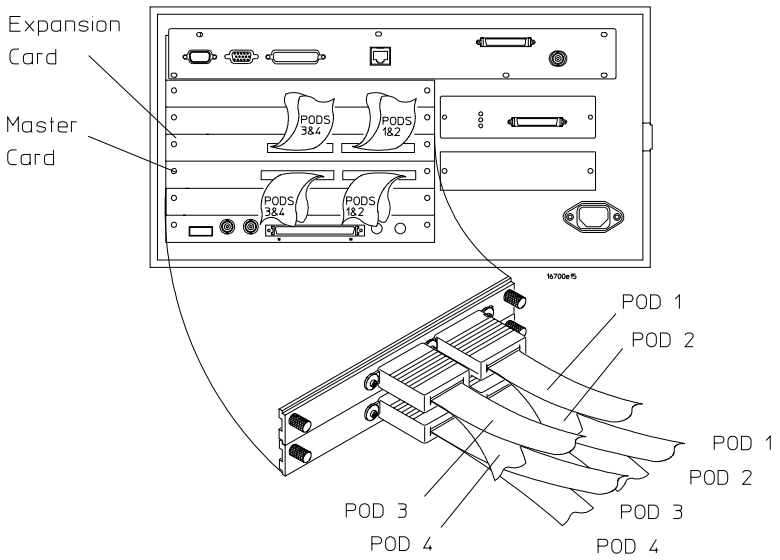
16550A Expansion Card	Expansion Card Pod 6	Expansion Card Pod 5	Expansion Card Pod 4	Expansion Card Pod 3	Expansion Card Pod 2	Expansion Card Pod 1
E2459A Connector	not used	not used	P8 jtag	P7 busarb	P6 STAT	P5 STAT

16550A Master Card	Master Card Pod 6	Master Card Pod 5	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
E2459A Connector	P4 DATA	P3 DATA	P2 ADDR clk ↑ (68040)	P1 ADDR clk ↑ (68060)	not used	not used

Configuration File
Use configuration files C040F2 or C060F2 for the two-card 16550A logic analyzers.

To connect to the 16554/55/56 logic analyzers

Use the figure and table below to connect the analysis probe to the 16554A/55A/56A and 16555D/56D logic analyzers.

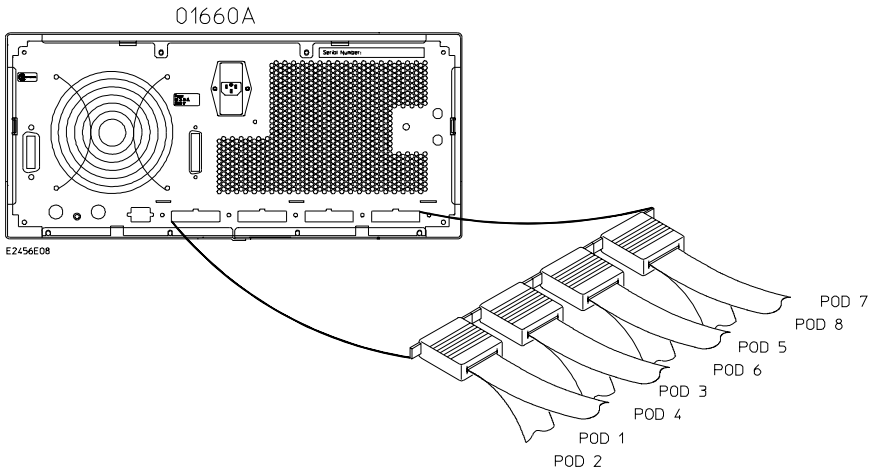


16554/55/56 Exp. Card 1	Expansion Card 1 Pod 4	Expansion Card 1 Pod 3	Expansion Card 1 Pod 2	Expansion Card 1 Pod 1
E2459A Connector	P8 jtag	P7 busarb	P6 STAT	P5 STAT
16554/55/56 Master Card	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
E2459A Connector	P4 DATA	P3 DATA	P2 ADDR clk ↑(68040)	P1 ADDR clk ↑(68060)

Configuration File
Use configuration files C040M or C060M for the 16554/55/56 logic analyzers.

To connect to the 1660A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the 1660A/C logic analyzers.

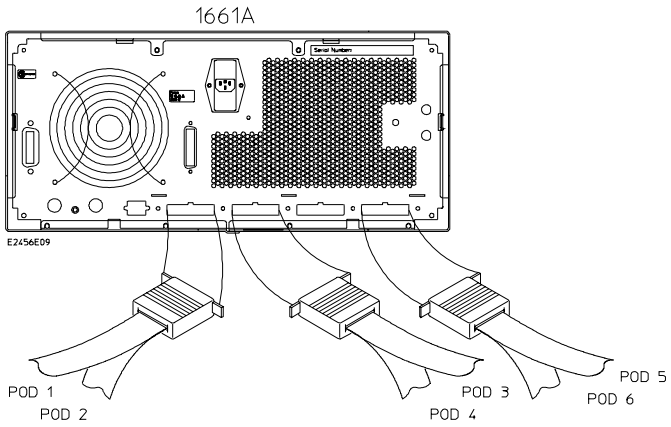


1660A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6	Pod 7	Pod 8
E2459A Connector	P1 ADDR clk ↑ (68060)	P2 ADDR clk ↑ (68040)	P3 DATA	P4 DATA	P5 STAT	P6 STAT	P7 busarb	P8 jtag

Configuration File
Use configuration files C040F2 or C060F2 for the 1660A/AS/C/CS/CP logic analyzers.

To connect to the 1661A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1661A/C logic analyzers.

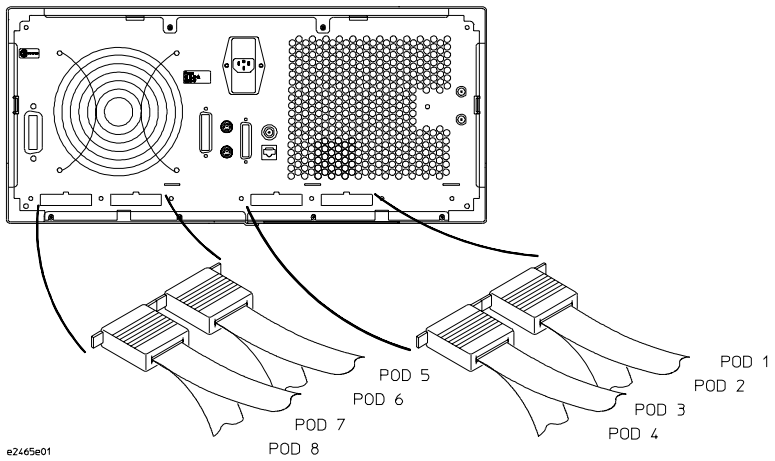


1661A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6
E2459A Connector	P1 ADDR clk ↑ (68060)	P2 ADDR clk ↑ (68040)	P3 DATA	P4 DATA	P5 STAT	P6 STAT

Configuration File
Use configuration files C040F2 or C060F2 for the 1661A/AS/C/CS/CP logic analyzers.

To connect to the 1670A/D logic analyzer

Use the figure and table below to connect the analysis probe to the 1670A/D logic analyzers.

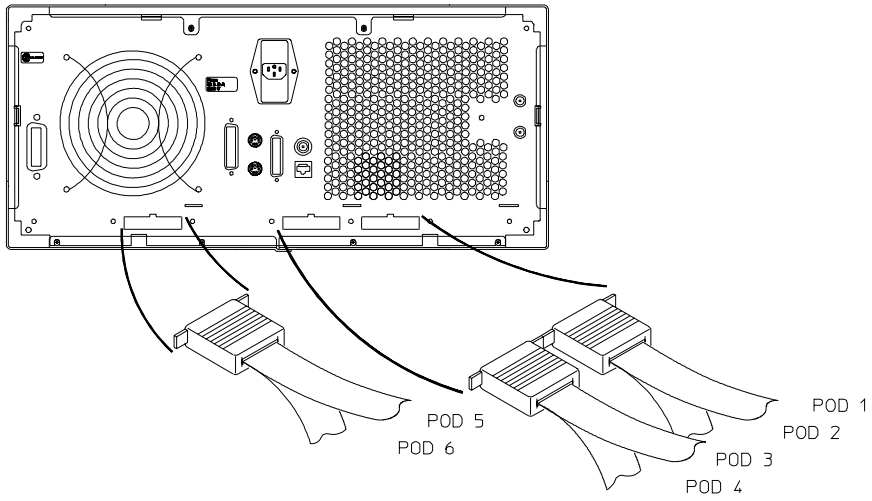


1670A/D	Pod 8	Pod 7	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
E2459A Connector	P8 jtag	P7 busarb	P6 STAT	P5 STAT	P4 DATA	P3 DATA	P2 ADDR clk ↑ (68040)	P1 ADDR clk ↑ (68060)

Configuration File
Use configuration files C040M3 or C060M3 for the 1670A/D logic analyzer.

To connect to the 1671A/D logic analyzer

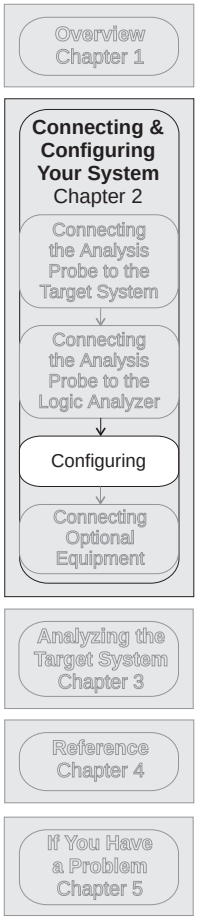
Use the figure and table below to connect the analysis probe to the HP 1671A/D logic analyzer.



1671A/D	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
E2459A Connector	P6 STAT	P5 STAT	P4 DATA	P3 DATA	P2 ADDR clk ↑ (68040)	P1 ADDR clk ↑ (68060)

Configuration File
Use configuration files C040M or C060M for the 1671A/D logic analyzer.

Configuring the Logic Analysis System



You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer
- Inverse assembler file name

The configuration file you use is determined by the logic analyzer you are using. The configuration file names are listed with the logic analyzer connection tables, and in a table at the end of this section.

The procedures for loading a configuration file depend on the type of logic analyzer you are using. There is one procedure for the 16600/700 series logic analysis systems, and another procedure for the 1660-series, 1670-series, and logic analyzer modules in an 16500B/C mainframe. Use the appropriate procedures for your analyzer.

To load configuration and inverse assembler files — 16600/700 logic analysis systems

If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

1 Click on the File Manager icon. Use File Manager to ensure that the subdirectory /logic/configs//m68040-060/ exists.

> If the above directory does not exist, you need to install the M68040-060 Processor Support Package. Close File Manager, then use the procedure on the CD-ROM jacket to install the M68040-060 Processor Support Package before you continue.

2 Using File Manager, select the configuration file you want to load in the /logic/configs//m68040-060/ directory, then click Load. If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

The logic analyzer is configured for 68040/060 analysis by loading the appropriate configuration file. Loading this file also automatically loads the appropriate inverse assembler.

3 Close File Manager.

To load configuration and inverse assembler files — other logic analyzers

If you have an 1660-series, 1670-series, or logic analyzer modules in an 16500B/C mainframe use these procedures to load the configuration file and inverse assembler.

The first time you set up the analysis probe, make a duplicate copy of the master disk. For information on duplicating disks, refer to the reference manual for your logic analyzer.

For logic analyzers that have a hard disk, you might want to create a directory such as 68040 on the hard drive and copy the contents of the floppy onto the hard drive. You can then use the hard drive for loading files.

1. Insert the floppy disk in the front disk drive of the logic analyzer.
2. Go to the Flexible Disk menu.
3. Configure the menu to load.
4. Use the knob to select the appropriate configuration file.

   Choosing the correct configuration file depends on which analyzer you are using. The configuration files are shown with the logic analyzer connection tables, and are also in the table on the next page.
5. Select the appropriate analyzer on the menu. The 16500 logic analyzer modules are shown in the Logic Analyzer Configuration Files table.
6. Execute the load operation on the menu to load the file into the logic analyzer.

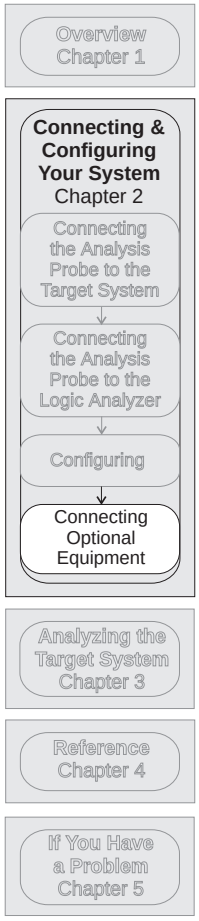
   The logic analyzer is configured for 68040 or 68060 analysis by loading the appropriate configuration file. Loading this file also automatically loads the appropriate inverse assembler.

Logic Analyzer Configuration Files

Analyzer Model	Analyzer Description (modules only)	Configuration File for 68040 Systems	Configuration File for 68060 Systems
16600A	na	C040F2	C060F2
16601A	na	C040F2	C060F2
16602A	na	C040F2	C060F2
16550A (one card)	100 MHz STATE 500 MHz TIMING	C040F	C060F
16550A (two card)	100 MHz STATE 500 MHz TIMING	C040F2	C060F2
16554A (two card)	0.5M SAMPLE 70/125 MHz LA	C040M	C060M
16555A (two card)	1.0M SAMPLE 110/250 MHz LA	C040M	C060M
16555D (two card)	2.0M SAMPLE 110/250 MHz LA	C040M	C060M
16556A (two card)	1.0M SAMPLE 100/200 MHz LA	C040M	C060M
16556D (two card)	2.0M SAMPLE 100/200 MHz LA	C040M	C060M
1660A/AS/C/CS	na	C040F2	C060F2
1661A/AS/C/CS	na	C040F2	C060F2
1670A/D	na	C040M3	C060M3
1671A/D	na	C040M	C060M

Connecting Optional Equipment

The E2459A does not support any additional equipment.



3

Analyzing the Target System

Analyzing the Target System

This chapter describes modes of operation for the E2459A analysis probe. It also describes analysis probe data, symbol encodings, and information about the inverse assemblers.

The information in this chapter is presented in the following sections:

- Modes of operation
- Logic analyzer configuration
- Using the inverse assemblers

Modes of Operation

The E2459A analysis probe provides three different analysis modes: State-per-transfer, State-per-clock, and Timing. The following sections describe these operating modes and how to configure the logic analyzer for each mode.

State-per-transfer mode

For State-per-transfer mode, the analyzers use the processor bus clock (BCLK for the 040, CLK for the 060) to strobe data. The configuration software sets up the trigger sequencer to filter out wait and idle states using store-qualification: only states "≠ idle" are stored. For the 68040s, the "idle" term is TA and TEA high (negated). For the 68060, it is TA, TEA, and TRA all high (negated).

For 68060 systems which use CLKEN to run the bus at 1/2 or 1/4 of the processor clock, CLKEN low (asserted) should be added to the storage qualification term. Note that this signal is only available in the eight-pod configurations, i.e., not on the 1661, 1671, or a one-card 16550A.

State-per-clock mode

In State-per-clock mode, every state is captured, including wait and idle states. For state-per-clock analysis, change the trigger sequence from 'Store "≠ idle"' to 'Store "anystate"'.

Timing mode

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1. **Select the Configuration menu of the logic analyzer.**
2. **Select the Type field for the analyzer and select Timing.**

   Timing data is displayed in the Waveform menu of the logic analyzer.

Logic Analyzer Configuration

The following sections describe the logic analyzer configuration as set up by the configuration files.

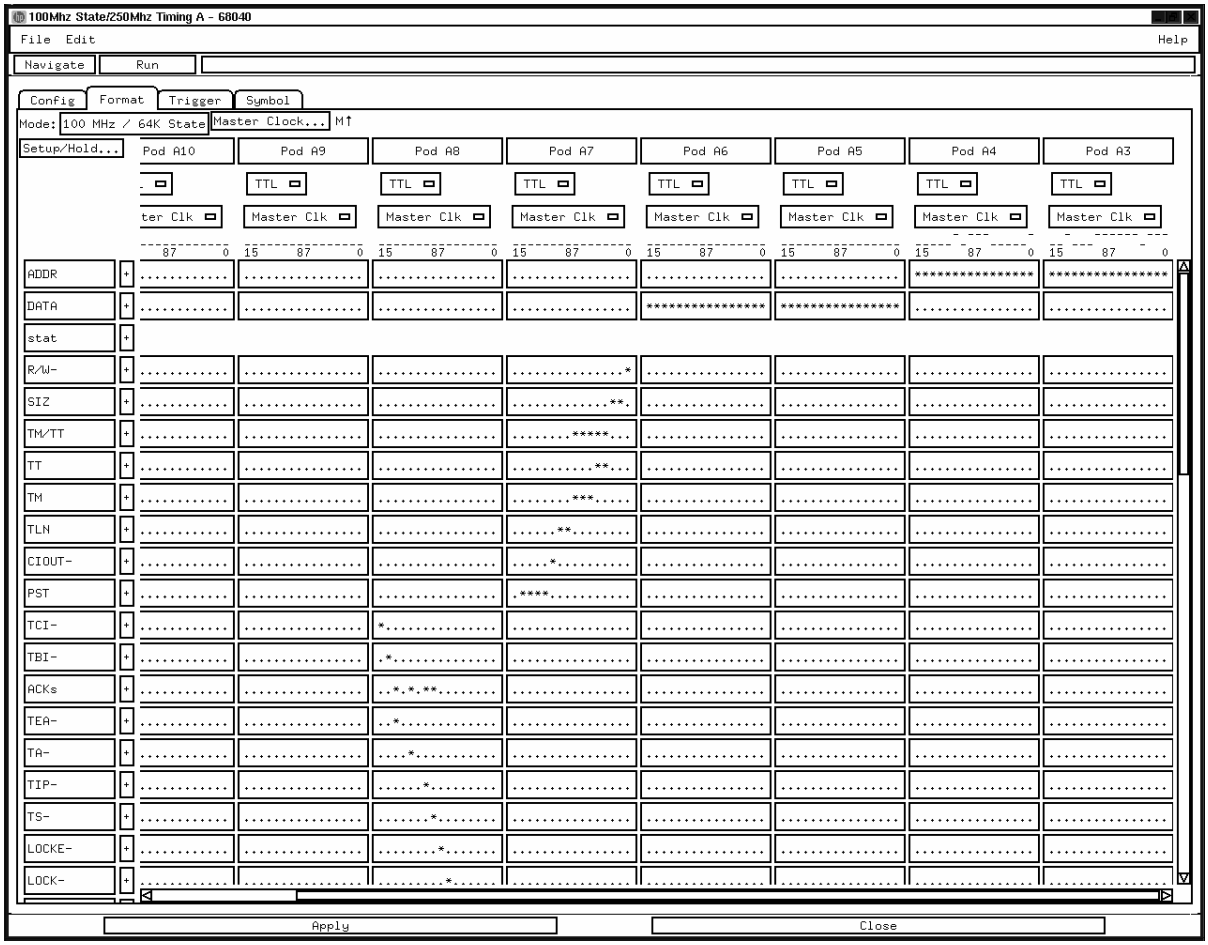
Trigger specification

The trigger specification is set up by the software to store all states. If you modify the trigger specification to store only selected bus cycles, you may get incorrect or incomplete disassembly.

Format specification

The configuration files contain predefined format specifications, shown in the figure on the following page. These format specifications include all labels for monitoring the microprocessor. The tables on the following pages show the signals used in the STAT label and the predefined symbols set up by the configuration files.

Do not modify the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changing these labels may cause incorrect or incomplete inverse assembly.



Format Specification

Status Encoding

Each of the bits of the STAT label is described in the table below. Bit 0 is the least significant bit of the 32-bit field.

Status Bit Definition

Bit	Status Signal	Description
0	R/W	This signal is high for read cycles and low for write cycles.
1-2	SIZ0-SIZ1	These signals indicate the size of the bus transfer requested by the microprocessor.
3-4	TT0-TT1	These signals encode the transfer type.
5-7	TM0-TM2	These signals are the transfer modifier signals which encode supervisor/user state, code/data access, and cache/MMU access.
27	TA	Transfer Acknowledge (TA) is low whenever the memory system has responded to a transfer.
29	TEA	Transfer Error Acknowledge (TEA) is set low to indicate the memory system failed to respond to a transfer.
24	TS	Transfer Start (TS) is brought low for the first clock cycle of a transfer.
25	TIP	Transfer in Process (TIP) is set low to indicate a transfer is in process.
28	TRA	Transfer Retry Acknowledge (TRA) (68060 only) is brought low to request a retry of the transfer.

Logic Analyzer Symbols

The E2459A configuration software sets up symbol tables on the logic analyzer. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

The following table lists the labels and symbol encodings defined by the logic analyzer configuration software.

Labels and Symbols

Label	Symbol	Status Encoding
R/W-	rd	1
R/W-	wr	0
SIZ	Long	0 0
SIZ	Byte	0 1
SIZ	Word	1 0
SIZ	Line	1 1
TM/TT	Cache Push	0 0 0 0 0
TM/TT	MMU Data	0 1 1 0 0
TM/TT	MMU Pgm	1 0 0 0 0
TM/TT	User Data	0 0 1 0 x
TM/TT	User Pgm	0 1 0 0 0
TM/TT	User	0 x x 0 x
TM/TT	Super Data	1 0 1 0 x
TM/TT	Super Pgm	1 1 0 0 0
TM/TT	Super	1 x x 0 x
TM/TT	Pgm	x 1 1 0 0
TM/TT	Data	x 0 1 0 x
TM/TT	Normal Acc	x x x 0 0
TM/TT	Move16 Acc	x x x 0 1
TM/TT	Alt FC 0	0 0 0 1 0
TM/TT	Debug Acc1	0 0 1 1 0
TM/TT	Reserved 2	0 1 0 1 0
TM/TT	Alt FC 3	0 1 1 1 0
TM/TT	Alt FC 4	1 0 0 1 0
TM/TT	Debug Pip5	10 1 1 0
TM/TT	Debug Pip6	11 0 1 0
TM/TT	Alt FC 7	1 1 1 1 0
TM/TT	Alt Access	x x x 1 0
TM/TT	Ack Access	x x x 1 1

Labels and Symbols

Label	Symbol	Status Encoding			
TT	Normal	0 0			
TT	Move16	0 1			
TT	Alt FC Access	1 0			
TT	Ack Access	1 1			
TM	Cache Push	0 0 0			
TM	MMU Data	0 1 1			
TM	MMU Pgm	1 0 0			
TM	User Data	0 0 1			
TM	User Pgm	0 1 0			
TM	User	0 x x			
TM	Super Data	1 0 1			
TM	Super Pgm	1 1 0			
TM	Super	1 x x			
TM	Pgm	x 1 0			
TM	Data	x 0 1			
CIOUT-		1			
CIOUT-	CI	0			
DATA_B	h Bxx	0110xxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
DATA_B	l Bxx	xxxxxxxx	xxxxxxxx	0110xxxx	xxxxxxxx
DATA_B	h Jxx	01001110	1xxxxxxx	xxxxxxxx	xxxxxxxx
DATA_B	l Jxx	xxxxxxxx	xxxxxxxx	01001110	1xxxxxxx
DATA_B	h RTx	01001110	01110xxx	xxxxxxxx	xxxxxxxx
DATA_B	l RTx'	xxxxxxxx	xxxxxxxx	01001110	01110xxx
DATA_B	h BSR	01100001	xxxxxxxx	xxxxxxxx	xxxxxxxx
DATA_B	l BSR	xxxxxxxx	xxxxxxxx	01100001	xxxxxxxx
DATA_B	h BRA	01100000	xxxxxxxx	xxxxxxxx	xxxxxxxx
DATA_B	l BRA	xxxxxxxx	xxxxxxxx	01100000	xxxxxxxx
DATA_B	h JSR	01001110	10xxxxxx	xxxxxxxx	xxxxxxxx
DATA_B	l JSR	xxxxxxxx	xxxxxxxx	01001110	10xxxxxx
DATA_B	h JMP	01001110	11xxxxxx	xxxxxxxx	xxxxxxxx
DATA_B	l JMP	xxxxxxxx	xxxxxxxx	01001110	11xxxxxx

Triggering

The analyzers use the processor bus clock (BCLK for the 040, CLK for the 060) to strobe data. The configuration software sets up the trigger sequencer to filter out wait and idle states using store-qualification: only states "≠ idle" are stored. For the 68040s, the "idle" term is TA and TEA high (negated). For the 68060, it is TA, TEA, and TRA all high (negated).

For State-per-clock analysis, change the trigger sequence from 'Store "≠ idle"' to 'Store "anystate"'.

For 68060 systems which use CLKEN to run the bus at 1/2 or 1/4 of the processor clock, CLKEN low (asserted) should be added to the storage qualification term. Note that this signal is only available in the eight-pod configurations, i.e., not on the 1661, 1671, or a one-card 16550A.

Trigger Menu

Using the Inverse Assembler

The E2459A analysis probe contains two inverse assemblers, I68040 and I68060. The appropriate inverse assembler is loaded by the configuration files.

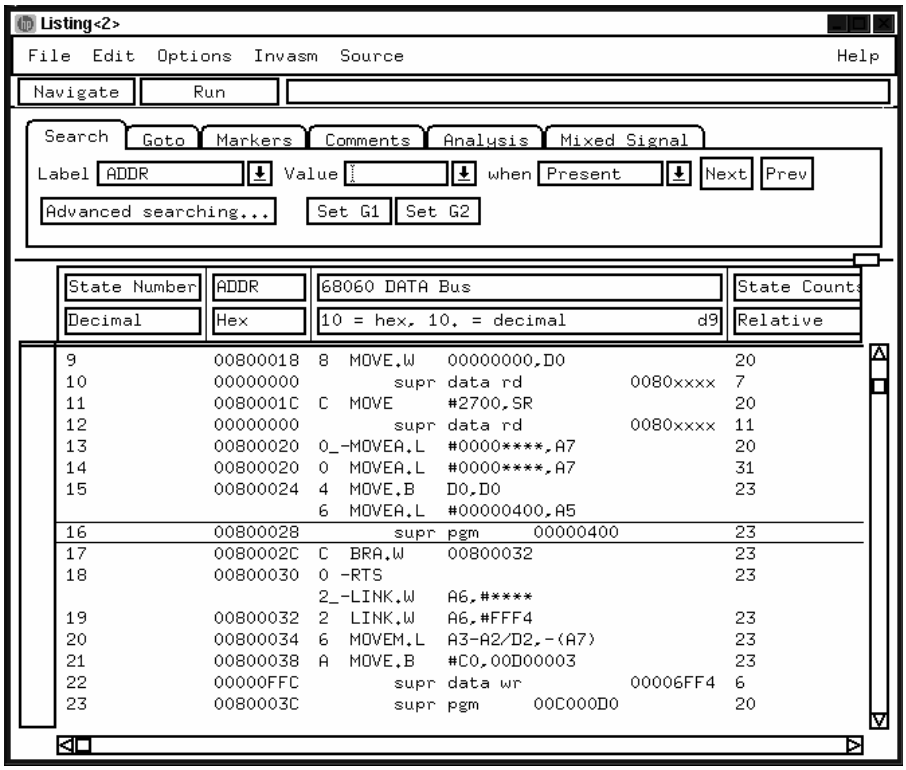
The following sections describe the features of the inverse assemblers.

For the 16600-series and 16700-series logic analysis systems, there are additional 68040 inverse assemblers on the hard drive. However, those additional 68040 inverse assemblers are for the E2420A Analysis Probe, and will not operate properly with the E2459A Analysis Probe. Do not load those inverse assemblers with this product.

Listing menu

Captured data is displayed as shown in the following figure. The figure displays the state listing for 32-bit bus cycles after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

The logic analyzer always probes the full 32-bit data bus of the 68040/040V/060. There are some memory systems that occasionally use only 8 or 16 bits for memory transactions. The size of the bus cycle is indicated by the SIZ signals from the microprocessor to the memory. When fewer than the full 32 bits of the data bus are used by a memory cycle, the inverse assembler marks the bits not used by the microprocessor with an "x".



Listing Menu

The "#" symbol in the state listing for the E2459A refers to an immediate operand.

Burst Data

During burst transfers, the microprocessor may hold the address bus constant during the entire burst. The disassembler calculates the address of each instruction, and displays the least significant hex digit in the left-hand column.

Interpreting data

Most numerical data presented by the disassembler is hexadecimal. An exception is bit numbers, which are displayed in decimal. Decimal output has a dot "." suffix. In general, asterisks indicate that the expected operand fetches were not stored in the logic analyzer memory. The pair of asterisks (**) displayed in the operand field of an instruction indicates that a byte of an expected operand was not stored in the logic analyzer memory. Four asterisks (****) indicate that one word of an expected operand was missing, and eight asterisks signify a missing long word. Missing operands (or parts of operands) can result from instruction prefetch activity, storage qualification, instruction cache operation, or address translation by the MMU.

Examples:

ORLB	#**,D2	(missing byte operand)
ORI.W	#****,D1	(missing word operand)
ORI.L	# 234A****,D3	(missing "lower" word of the operand)
ORI.L	# ********,D3	(missing both words of the operand)

The 68040/040V/060 microprocessors are capable of supporting byte, word, and long word (32-bit) operands. During operand reads and writes, entire 32-bit values appear on the microprocessor data bus. In the case of single-byte operands, the inverse assembler will display "xx" for the bytes of the input data that are ignored by the microprocessor. In this manner, it is possible to determine exactly which byte of data the microprocessor has used as an operand.

There is a chance that two instructions (16 bits each) will be fetched on one bus cycle. When this happens, the instructions will be displayed on separate lines.

The 68040/040V/060 microprocessors are prefetching microprocessors. That is, they will fetch subsequent instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, the prefetched words are not used and will be discarded by the microprocessor. These words are referred to as "overfetch."

The logic analyzer captures prefetches, even if they are not executed. Therefore, care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

When the inverse assembler detects a change in the sequential address flow, it will prepend an underscore, "_", to indicate the break.

To align the inverse assembler

The 68040/040V/060 microprocessors do not provide enough status information for the inverse assemblers to pick out the first word of an opcode fetch from a series of program reads. To ensure correct disassembly, you may need to point to the 16-bit word that contains the first word of an opcode fetch. Once aligned, the inverse assembler will disassemble from this state through the end of the screen.

Use the following procedure to align the inverse assembler:

1. Select a line on the display that you know contains the first word of an opcode fetch.
2. Roll this line to the top of the display.

> Do not roll the instruction to the line number field at the left center screen. In the Listing Menu figure on page 3-11, line 9 is the top of the display.

3. Select the appropriate field for your analyzer.
   a. For the 16600/700 series analyzers, select "Invasm," then select "Align." A pop-up menu appears with the following choices:

      ```
      High Word
      Low Word
      ```

   b. For the other logic analyzers, select "Invasm Options" and use the "Code Synchronization" submenu. The same choices as above are available.
4. Select the choice that identifies which word of the 32-bit long word contains the first word of the instruction fetch, then select "Align."

   The listing inverse assembles from the top line down. Any data before the top of the display is left unchanged.

   Rolling the display up inverse assembles the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may need to re-align the inverse assembler by repeating steps 1 through 4.

   Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble

several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

The 68040 inverse assembler may lose synchronization due to jumps and branches to odd word addresses. When this occurs, re-synchronize the inverse assembler by repeating steps 1 through 4.

Overfetch marking

The inverse assemblers attempt to mark unused program fetches. Overfetch arises from two sources:

- Cache line wrap. This occurs when a cache line is fetched and the first long word is not at an address which is a multiple of 16. For example, if the fetch sequence is 8, C, 0, 4, then the long words at 0 and 4 are not in the sequential execution path. These words are marked with an asterisk, "*".
- Instructions and exceptions which flush the pipeline in the instruction fetch unit. Pipeline flushes caused by instructions are marked with a hyphen, "-" or a question mark, "?" in decreasing order of reliability.

There are two prerequisites for reliable detection of instruction-caused overfetch:

- Instruction execution is a subset of bus activity captured by the logic analyzer; that is, the instruction cache is disabled and the analyzer is not excluding program fetches due to store-qualification.
- The logical addresses used on the microprocessor correspond to the physical addresses seen on the bus; that is, the MMU is not performing any address translation.

See the next section for more information on disabling the cache and MMU. There are five categories of instruction which may cause overfetch:

- The following instructions flush and refill the pipeline, without upsetting the orderly flow of instruction execution:

nop (68040 only)		
move	ea , SR	
movec	Rn , Rc	
fmove	FPcr	(either way)
fmovem		(data or control)
cinv		

- The following instructions flush the pipeline and refill it from the target address:

```
bra     targ
bsr     targ
jmp     <eak>
jsr     <eak>
```

  <eak> (effective address known) is one of the addressing modes where the target is known:

  xxxx.W

  xxxxxxxx.L

  xxxx(PC)

- The following instructions may be somewhat ambiguous. They may or may not behave like a branch.

```
bcc     targ
dbcc    targ
```

- The following instructions flush the pipeline and refill it from a target address that is not known by the inverse assembler:

```
jsr     <eau>
jmp     <eau>
rtd     # xxxx
rte
rtr
stop    # xxxx
rts
trap    # n
```

  <eau> (effective address unknown) is any addressing mode other than <eak>.

  The rts and trap instructions are similar to jmp <eau>, but the inverse assembler may be able to determine the branch address if data transactions on the bus are not filtered out by storage qualification.

- The following instructions may act like a trap instruction:

  trapcc

  trapv

Disabling the cache and MMU

The logic analyzer captures bus activity; when the processor's instruction cache is enabled, not all program activity is visible on the bus. If you need a complete execution trace, disable the instruction cache to force all instruction fetches to come in on the bus. This can be accomplished in various ways:

- The target hardware asserts TCI (transfer cache inhibit)
- The target software disables the instruction cache by clearing bit 15 (instruction cache enable) in the cache control register. For example:

```
MOVE.L   #80000000, D0          # enable data, disable
MOVEC    D0, CACR               # instruction cache
```

The instruction MMU is programmed to use non-cachable transparent translation for the code space.

If you are using the disassembler and are attempting to trace branch flow, you may wish to configure the Memory Management Unit (MMU) so that the physical addresses the analysis probe monitors are the same as the logical addresses that the processor uses. This can be done by clearing bit 15 of the translation control register. For example:

```
MOVEQ    #0, D0                 # disable MMU
MOVEC    D0, TCR                # translation
```

(The 68EC040 and 68EC060 do not have an MMU, so this is not an issue for those processors.)

Inverse assembler error messages

Any of the following error messages may appear during analysis of your target software. Included with each message is a brief explanation.

Data Error

Trace data collected by the logic analyzer cannot be retrieved from memory. This indicates a hardware error or inverse assembler software error.

Illegal Opcode

Undefined opcode encountered. Microprocessor action cannot be determined.

4

Reference

Reference

This chapter contains additional reference information including the signal mapping for the E2459A Analysis Probe.

The information in this chapter is presented in the following sections:

- Operating characteristics of the analysis probe
- Theory of operation and clocking
- Signal-to-connector mapping
- Circuit board dimensions
- Replaceable parts

Operating characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the analysis probe.

Product Characteristics	
Microcontrollers Supported	Motorola 68040, 68EC040, 68LC040, 68040V, 68EC040V, 68060, 68EC060, and 68LC060.
Package Supported	179-pin PGA for the 68040, 68EC040, and 68LC040. 184-pin PQFP for the 68EC040 and 68LC040. 182-pin PGA for the 68040V and 68EC040V. 184-pin PQFP for the 68040V and 68EC040V. 206-pin PGA for the 68060, 68EC060 and 68LC060.
Accessories Required	E5345A for 184-pin PQFP target systems.
Logic Analyzer Required	1660A/AS/C/CS/CP, 1661A/AS/C/CS/CP, 1670A/D, 1671A/D, 16550A (one or two cards), 16554/55/56 (two cards), 16600/01/02.
Number of Probes Used	Up to eight 16-channel pods. Six pods are required for inverse assembly.
Microprocessor Operations Displayed	Burst Transfer User Data Read/Write User Program Read Supervisor Read/Write Supervisor Program Read CPU Space Accesses including Breakpoint Acknowledge and Interrupt Acknowledge.
Additional Capabilities	The logic analyzer captures all bus cycles.
Power Requirements	None.
Signal Line Loading	100 Kohms.
Maximum Clock Speed	66 MHz Clock Input.
Environmental Characteristics	This product is intended for indoor use only.
Temperature	Operating: 0 to + 55 degrees C (+32 to +131 degrees F) Nonoperating: -40 to + 75 degrees C (-40 to +167 degrees F)
Altitude	Operating: 4,600 m (15,000 feet) Nonoperating: 15,3000 m (50,000 feet)
Humidity	Up to 90% noncondensing. Avoid sudden , extreme temperature changes which could cause condensation on the circuit board.

Theory of operation and clocking

The following section provides information regarding the timing, clocking, and signal mapping of the Agilent E2459A Analysis Probe.

Target Signal Timing

The logic analyzers require a 3.5 ns of combined setup and hold time relative to the analyzer clock.

Clocking

Three clocking sources are available.

- Test clock (TCK) is used to clock data into/out of the microprocessor's JTAG interface. This signal is available for all microprocessors.
- Bus Clock (BCLK) is one half the system clock frequency and is available on the 68040 and 68040V.
- Processor clock (PCLK or CLK) is the system clock frequency. This is the reference used for internal CPU timing. PCLK/CLK is available for the 68040 and 68060 microprocessors.

Signal-to-connector mapping

The following table shows the electrical interconnections implemented with the analysis probe.

MC68040/040V/060 Signal List

PIN	PIN NAME	USED ON 040	040V	060	E2459A CABLE	E2459A CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
L18	A0	x	x	x	1	37	0	ADDR
K18	A1	x	x	x	1	35	1	ADDR
J17	A2	x	x	x	1	33	2	ADDR
J18	A3	x	x	x	1	31	3	ADDR
H18	A4	x	x	x	1	29	4	ADDR
G18	A5	x	x	x	1	27	5	ADDR
G16	A6	x	x	x	1	25	6	ADDR
F18	A7	x	x	x	1	23	7	ADDR
E18	A8	x	x	x	1	21	8	ADDR
F16	A9	x	x	x	1	19	9	ADDR
P1	A10	x	x	x	1	17	10	ADDR
N3	A11	x	x	x	1	15	11	ADDR
N1	A12	x	x	x	1	13	12	ADDR
M1	A13	x	x	x	1	11	13	ADDR
L1	A14	x	x	x	1	9	14	ADDR
K1	A15	x	x	x	1	7	15	ADDR
R9	PCLK	x			1	3	CLK	
R9	JS2		x		1	3	CLK	
R9	CLK			x	1	3	CLK	

PIN	PIN NAME	USED ON 040	040V	060	E2459A CABLE	E2459A CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
K2	A16	x	x	x	2	37	0	ADDR
J1	A17	x	x	x	2	35	1	ADDR
H1	A18	x	x	x	2	33	2	ADDR
J2	A19	x	x	x	2	31	3	ADDR
G1	A20	x	x	x	2	29	4	ADDR
F1	A21	x	x	x	2	27	5	ADDR
E1	A22	x	x	x	2	25	6	ADDR
G3	A23	x	x	x	2	23	7	ADDR
D1	A24	x	x	x	2	21	8	ADDR
F3	A25	x	x	x	2	19	9	ADDR
E2	A26	x	x	x	2	17	10	ADDR
C1	A27	x	x	x	2	15	11	ADDR
E3	A28	x	x	x	2	13	12	ADDR
B1	A29	x	x	x	2	11	13	ADDR
D3	A30	x	x	x	2	9	14	ADDR
A1	A31	x	x	x	2	7	15	ADDR
R7	BCLK	x	x		2	3	CLK	
C3	D0	x	x	x	3	37	0	DATA
B3	D1	x	x	x	3	35	1	DATA
C4	D2	x	x	x	3	33	2	DATA
A2	D3	x	x	x	3	31	3	DATA
A3	D4	x	x	x	3	29	4	DATA
A4	D5	x	x	x	3	27	5	DATA
A5	D6	x	x	x	3	25	6	DATA
A6	D7	x	x	x	3	23	7	DATA

PIN	PIN NAME	USED ON 040	040V	060	E2459A CABLE	E2459A CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
B7	D8	x	x	x	3	21	8	DATA
A7	D9	x	x	x	3	19	9	DATA
A8	D10	x	x	x	3	17	10	DATA
A9	D11	x	x	x	3	15	11	DATA
A10	D12	x	x	x	3	13	12	DATA
A11	D13	x	x	x	3	11	13	DATA
A12	D14	x	x	x	3	9	14	DATA
A13	D15	x	x	x	3	7	15	DATA
S4	TCK	x	x	x	3	3	CLK	CLK
B11	D16	x	x	x	4	37	0	DATA
A14	D17	x	x	x	4	35	1	DATA
B12	D18	x	x	x	4	33	2	DATA
A15	D19	x	x	x	4	31	3	DATA
A16	D20	x	x	x	4	29	4	DATA
A17	D21	x	x	x	4	27	5	DATA
B16	D22	x	x	x	4	25	6	DATA
C15	D23	x	x	x	4	23	7	DATA
A18	D24	x	x	x	4	21	8	DATA
C16	D25	x	x	x	4	19	9	DATA
B18	D26	x	x	x	4	17	10	DATA
D16	D27	x	x	x	4	15	11	DATA
C18	D28	x	x	x	4	13	12	DATA
E16	D29	x	x	x	4	11	13	DATA
E17	D30	x	x	x	4	9	14	DATA
D18	D31	x	x	x	4	7	15	DATA

PIN	PIN NAME	USED ON 040	040V	060	E2459A CABLE	E2459A CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
N16	R/W	x	x	x	5	37	0	STAT
P17	SIZ0	x	x	x	5	35	1	STAT
P16	SIZ1	x	x	x	5	33	2	STAT
P3	TT0	x	x	x	5	31	3	STAT
P2	TT1	x	x	x	5	29	4	STAT
N18	TM0	x	x	x	5	27	5	STAT
M18	TM1	x	x	x	5	25	6	STAT
K17	TM2	x	x	x	5	23	7	STAT
Q18	TLN0	x	x	x	5	21	8	STAT
P18	TLN1	x	x	x	5	19	9	STAT
R1	CIOUT	x	x	x	5	17	10	STAT
T15	PST0	x	x	x	5	15	11	STAT
S14	PST1	x	x	x	5	13	12	STAT
R14	PST2	x	x	x	5	11	13	STAT
T16	PST3	x	x	x	5	9	14	STAT
Q13	PST4			x	5	7	15	STAT
Q4	BS0			x	6	37	0	STAT
Q5	BS1			x	6	35	1	STAT
Q6	BS2			x	6	33	2	STAT
Q7	BS3			x	6	31	3	STAT
Q3	UPA0	x	x	x	6	29	4	STAT
Q1	UPA1	x	x	x	6	27	5	STAT
S18	LOCK	x	x	x	6	25	6	STAT
R18	LOCKE	x	x	x	6	23	7	STAT

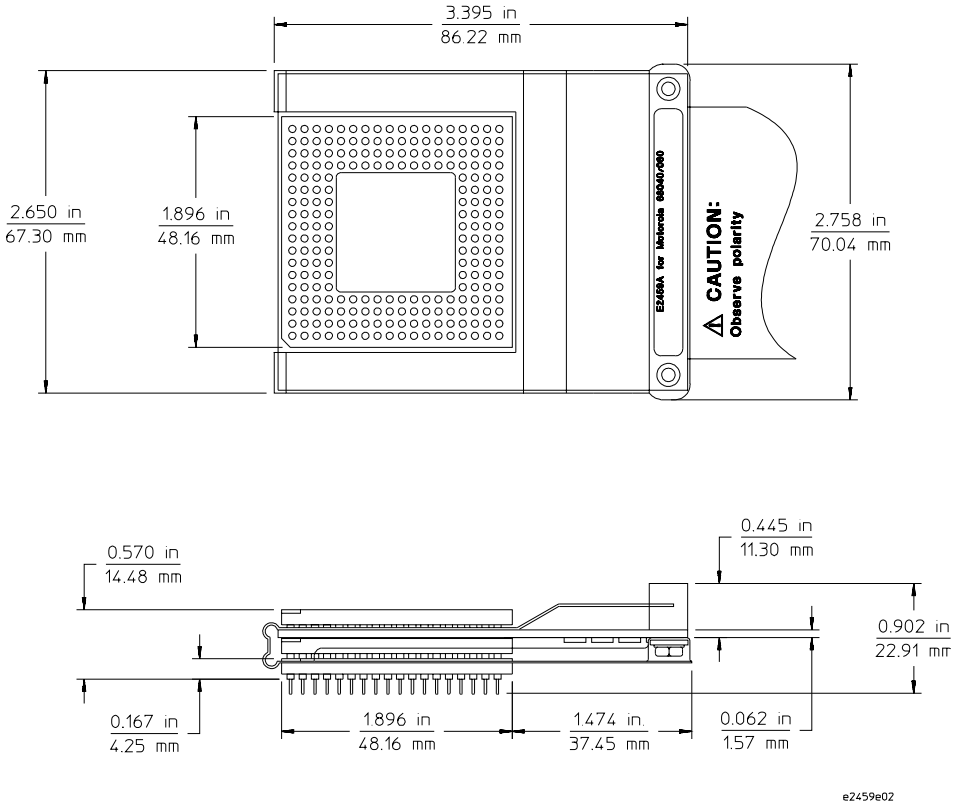
PIN	PIN NAME	USED ON 040	040V	060	E2459A CABLE	E2459A CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
R16	TS	x	x	x	6	21	8	STAT
R15	TIP	x	x	x	6	19	9	STAT
Q14	SAS			x	6	17	10	STAT
T14	TA	x	x	x	6	15	11	STAT
Q12	TRA			x	6	13	12	STAT
S13	TEA	x	x	x	6	11	13	STAT
S11	TBI	x	x	x	6	9	14	STAT
T10	TCI	x	x	x	6	7	15	STAT
T9	DLE*	x	x		7	37	0	
T12	SC0	x	x		7	35	1	
S12	SC1	x	x		7	33	2	
Q16	MI	x	x		7	31	3	
P15	SNOOP			x	7	29	4	
K15	CLA			x	7	27	5	
T18	BR	x	x	x	7	25	6	
T13	BG	x	x	x	7	23	7	
Q11	BGR			x	7	21	8	
T17	BB	x	x	x	7	19	9	
Q15	BTT			x	7	17	10	
T8	IPL0	x	x	x	7	15	11	
T7	IPL1	x	x	x	7	13	12	
T6	IPL2	x	x	x	7	11	13	
S1	IPEND	x	x	x	7	9	14	
T11	AVEC	x	x	x	7	7	15	

PIN	PIN NAME	USED ON 040	040V	060	E2459A CABLE	E2459A CONNECTOR PIN	ANALYZER BIT	TIMING LABEL
T5	CDIS	x	x	x	8	37	0	
S6	MDIS**	x	x	x	8	35	1	
S7	RSTI	x	x	x	8	33	2	
R3	RSTO	x	x	x	8	31	3	
T3	TRST	x		x	8	29	4	
T4	JTAG			x	8	27	5	
S5	TMS	x	x	x	8	25	6	
S3	TDI	x	x	x	8	23	7	
T2	TDO	x	x	x	8	21	8	
D4	LFO		x		8	19	9	
K4	LOC		x		8	17	10	
M4	SCD		x		8	15	11	
Q8	CLKEN			x	8	13	12	
						11	13	
						9	14	
						7	15	

* On the 68EC040, 68LC040, 68040V, and 68EC040V, this signal is called JSO.
** On the 68EC040 and 68EC040V, this signal is called JS1.

Circuit board dimensions

The following figure gives the dimensions for the analysis probe. The dimensions are listed in inches and millimeters.



Dimensions

Replaceable parts

The repair strategy for this analysis probe is board replacement. However, the table below lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Agilent Sales Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Agilent. These assemblies have been set up on the "Exchange Assembly" program. This lets you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

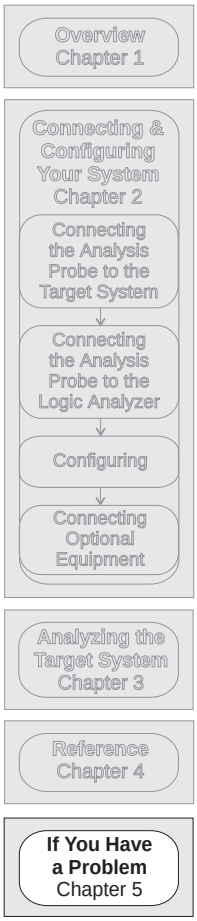
Replaceable Parts

Agilent Part Number	Description
E2459-66501	Circuit board assembly
E2459-68700	Inverse assembler disk pouch
E2459-44101	ESD Cover
1200-1908	Pin protector IC socket (182-pin 68040V footprint)
1200-1906	Pin protector IC socket (206-pin 68060 footprint)
1200-1910	Pin protector IC socket (179-pin 68040 footprint)
E5345A	184-pin PQFP probe adapter

5

If You Have a Problem

If You Have a Problem



Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages
- Cleaning the instrument

If you still have difficulty after trying the suggestions in this chapter, contact your local Agilent Service Center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and analysis probe connections.
- ☐ Check for bent or damaged pins on the analysis probe.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your trigger sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analyzer won't power up

If the logic analyzer power is powered down when it is connected to a powered-up target system, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system that is already powered up.

- ☐ Disconnect all logic analyzer cabling from the analysis probe. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Agilent Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the analysis probe and target system.**

  1 Power up the analyzer and analysis probe.

  2 Power up the target system.

  If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the analysis probe are properly rotated and aligned so that the index pin on the microprocessor (pin 1 or pin A1) matches the index pin on the analysis probe.**

- ☐ **Verify that the microprocessor and the analysis probe are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.**

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some analysis probe designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.**

  See “Capacitive Loading” in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

  Some microprocessors generate substantial heat. This is exacerbated by the active circuitry on the analysis probe board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ☐ **Remove as many pin protectors, extenders, and adapters as possible.**

- ☐ **If multiple analysis probe solutions are available, use one with lower capacitive loading.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the analysis probe or in your target system. If you follow the suggestions in this section to ensure that you are using the analysis probe and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect alignment, modified configuration files, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ☐ **Ensure that each logic analyzer pod is connected to the correct analysis probe connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and analysis probe cable numbers. Microprocessor interfaces must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each analysis probe are often altered to support that need. Thus, one analysis probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 2 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. See Chapter 3 for more information.

- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **For the 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM. Re-install the Processor Support Package for this product, then try loading the configuration file again.**

- ☐ **For other logic analyzers, ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler, rename it, or use the File Manager Copy command to copy it to the 16600/700 logic analysis systems, the configuration process will fail to load the inverse assembler.

  See Chapter 3 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- ☐ **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- ☐ **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger condition one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and may not always be related to the event you are trying to capture with the oscilloscope.

Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Enhanced Inverse Assembler Not Found"

This error only occurs on the 16600/700 logic analysis systems. This error occurs if you rename or delete the enhanced inverse assembler file that is attached to the configuration file, or if you do not properly install the inverse assembler file on the hard disk. Ensure that the inverse assembler file is not renamed or deleted. If you use the File Manager Copy command to copy an inverse assembler to the 16600/700 logic analysis systems, the enhanced inverse assembler will not load. Use the Install procedures listed on the jacket of the CD ROM to install the files for this product.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

For the 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM.

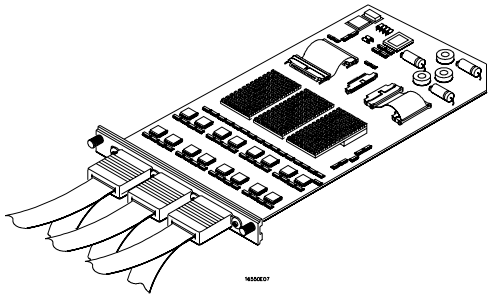
For other logic analyzers, if you have copied the files to the logic analyzer hard disk, ensure that the inverse assembler is located in the same directory as the configuration file.

". . . Does Not Appear to be an Inverse Assembler File"

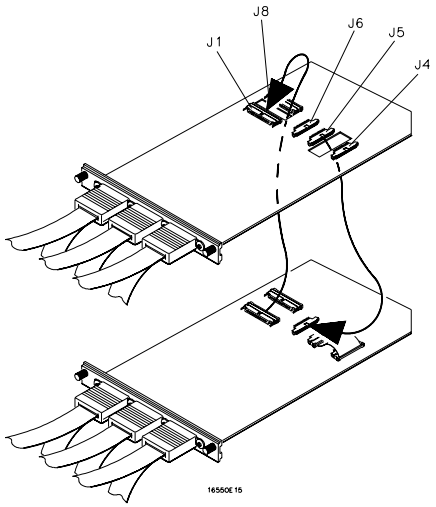
This error occurs if the inverse assembler file requested by the configuration file is not a valid inverse assembler. Use the Install procedures listed on the jacket of the CD ROM to re-install the files for this product.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly on logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card 16550A installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card 16550A Installations

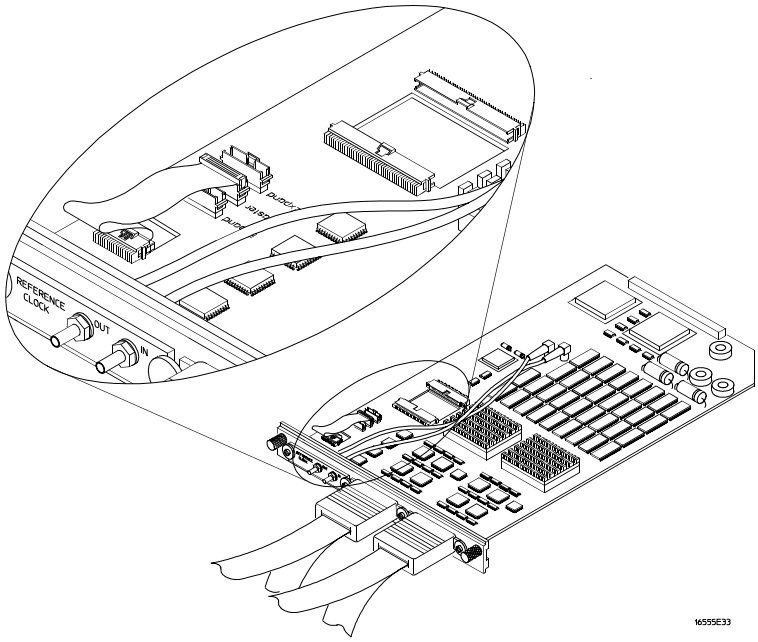


Cable Connections for Two-Card 16550A Installations

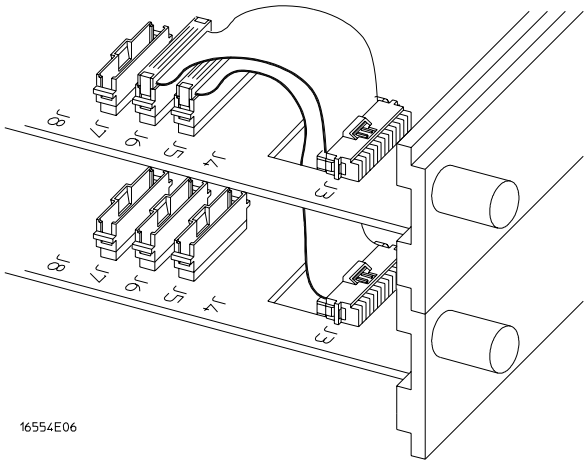
See Also

The *16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

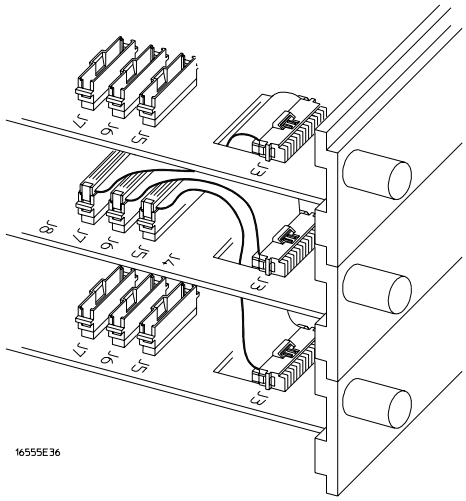
The following diagrams show the correct cable connections for one-card, two-card, and three-card installations on 16554A, 16555A/D, and 16556A/D logic analysis cards. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card 16554/55/56 Installations



Cable Connections for Two-Card 16554/55/56 Installations



Cable Connections for Three-Card 16554/55/56 Installations

See Also

The 16554A 70-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The 16555A 110-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The 16556A 100-MHz State/400-MHz Timing Logic Analyzer Service Guide.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the 16500A/B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

See Also Chapter 2 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system mainframe. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe. See Chapter 2 to determine the proper connections.

"Time from Arm Greater Than 41.93 ms"

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

Glossary

Analysis Probe A probe connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer.

Connector Board A board whose only function is to provide connections from one location to another. One or more connector boards might be stacked to raise a probe above a target micoprocessor to avoid mechanical contact with other components installed close to the target microprocessor.

Elastomeric Probe Adapter A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

Emulation Module An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Probe.

Emulation Probe An emulation probe is a stand-alone instrument connected to the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Module.

Flexible Adapter Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

General-purpose Flexible Adapter A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

High-Density Adapter Cable A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High Density Termination Adapter Cable Same as a High Density Adapter Cable, except it has a termination in the Mictor connector.

Jumper Moveable direct electrical connection between two points.

Mainframe Logic Analyzer A logic analyzer that resides on one or more board assemblies installed in an 16500B/C, 1660xA, or 16700A mainframe.

Male-to-male Header A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

Preprocessor Interface See Analysis Probe.

Preprocessor Probe See Analysis Probe.

Probe adapter See Elastomeric Probe Adapter.

Processor Probe See Emulation Probe and Emulation Module.

Prototype Analyzer The 16505A prototype analyzer acts as an analysis and display processor for the 16500B/C logic analysis system. It provides a windowed interface and powerful analysis capabilities.

Setup Assistant A software program that guides you through the process of connecting and configuring an analysis probe and logic analyzer to make measurements on a specific microprocessor.

Shunt Connector. See Jumper.

Stand-alone Logic Analyzer A stand-alone logic analyzer has a predefined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A stand-alone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

Transition Board A board assembly that obtains signals connected to one side and re-arranges them in a different order for delivery at the other side of the board.

1/4-Flexible Adapter An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

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